IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] Cross Reference to Related ~~Application:~~ Applications: This application is a continuation of application Serial No. 09/518,293, filed March 3, 2000, ~~pending~~ now U.S. Patent 6,287,942, issued September 11, 2001, which is a continuation of application Serial No. 09/244,733, filed February 5, 1999, now U.S. Patent 6,084,288, issued July 4, 2000, which is continuation of application Serial No. 08/910,613, filed August 13, 1997, now U.S. Patent 5,903,044, issued May 11, 1999, which is a continuation of application Serial No. 08/614,178, filed March 12, 1996, now U.S. Patent 5,682,065, issued October 28, 1997.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] Referring initially to drawing Fig. 5, a portion of a silicon substrate wafer 10 is shown having portions of two semiconductor chips 12 formed thereon, each semiconductor chip 12 having, in turn, bond pads 14 thereon, passivation layers 18 thereon, circuitry 20 therein, and street areas 22 located between the semiconductor chips 12 formed on the wafer 10. Initially, while the semiconductor chips 12 are in the form of a wafer 10, the active circuitry side of the semiconductor chips 12, i.e., the top or first side of the wafer 10, is coated with suitable etchable glass ~~coating~~ layer 30 of sufficient thickness to cover the wafer 10 in its entirety including the street areas 22 formed between the adjacent semiconductor chips 12 on the wafer 10 while maintaining the surface of the wafer 10 in a substantially planar state. The glass ~~coating~~ layer 30 of etchable glass may be added to the wafer 10 by any suitable well known technique, such as spin coating, dip or flow coating. It is preferable that the etchable glass coating be a type of glass that cures at a relatively low temperature, such as curing at a temperature generally less than six hundred degrees Centigrade (600° C) and is easily etched in subsequent etching processes. Such types of etchable glasses are well known and may be selected depending upon processing convenience during manufacture.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] Referring to drawing Fig. 7, as shown in the next step of the method of the present invention, a suitable resist material (not shown) is applied using well known conventional techniques to the bottom or second side of the wafer 10 with the street areas 22 located between the semiconductor chips 12 of the wafer 10 being subsequently etched through to the etchable glass ~~coating~~ layer 30 applied to the top or first side of the wafer 10. In this manner, the semiconductor chips 12 are separated from each other while being retained in the form of a wafer 10 by the etchable glass ~~coating~~ layer 30 on the top side of the wafer 10. If hard masking techniques are used to apply the suitable resist material, the resist need not be removed from the back side of the wafer 10 after the wafer 10 is etched through to the etchable glass ~~coating~~ layer 30. Conversely, if polymeric types of masking techniques are used to apply the suitable resist material, the resist should be removed after the etching of the wafer 10.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] Referring to drawing Fig. 8, after the removal of the resist coating, the next step in the method of the present invention is to apply a suitable etchable glass coating 40 to the bottom or second side of the semiconductor chips 12 formed on the wafer 10 to uniformly coat the bottom or second sides of the semiconductor chips 12 and fill the etched portions of the street areas 22 located between the semiconductor chips 12 of the wafer 10. The etchable glass coating 40 may be of any suitable material and applied by any suitable manner as described hereinbefore. After the application of the glass coating 40 of etchable glass to semiconductor chips 12, the semiconductor chips 12 effectively remain in the form of a wafer 10 by the glass ~~coatings~~ layer 30 and the glass coating 40 reforming the wafer 10 by filling the street areas 22 previously etched between the semiconductor chips 12 and coating both the top and bottom, first and second sides, of the wafer 10.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] Referring to drawing Fig. 9, the next step of the method of the present invention comprises applying a suitable resist material (not shown) to the glass ~~coating~~ layer 30 and etching the glass ~~coating~~ layer 30 through to expose the bond pads 14 of the semiconductor chips 12. In this manner, the bond pads 14 of the individual semiconductor chips 12 are exposed to have suitable connections made thereto.

Please replace paragraph number **[0038]** with the following rewritten paragraph:

[0038] Referring to drawing Fig. 10, the next steps in the method of the present invention are (1) forming a suitable metal coating on the glass ~~coating~~ layer 30 to substantially hermetically seal the areas of the glass ~~coating~~ layer 30 etched to expose the bond pads 14 of the semiconductor chips 12 and to form suitable electrical connections to the bond pads 14, (2) applying a suitable resist coating (not shown) to the metal coating on the glass ~~coating~~ layer 30 having the desired circuitry 16 to connect the bond pads 14 to a predetermined desired connector (not shown), and (3) etching the metal coating to yield the desired circuitry connections 16 (see drawing Figs. 2 through 4) to the bond pads 14 of each semiconductor chip 12. Subsequent to the circuitry 16 being formed on the surface of the glass ~~coating~~ layer 30 to form a substantially hermetical seal and to form connections with the bond pads 14 of semiconductor chips 12, the resist coating is removed from the circuits 16 and the individual semiconductor chips 12 are separated by sawing, severing, dividing or cutting the street areas 22 between each semiconductor chip 12 as shown at cuts 50. The cuts 50 are made in the street areas 22 so that portions of the glass ~~coatings~~ layer 30 and the glass coating 40 remain in substantial contact with each edge of each semiconductor chip 12, thereby substantially hermetically sealing all edges of each semiconductor chip 12. In this manner, each semiconductor chip 12 is substantially fully hermetically sealed on the top, bottom, and all edges thereof by the glass ~~coatings~~ layer 30 and the glass coating 40 and metal circuits 16 connected to bond pads 14, thereby leaving no portion of the semiconductor chip 12 exposed for any environmental attack thereto.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] Referring to drawing Fig. 11, shown connected to a conventional lead frame 60 is a portion of a semiconductor chip 12 substantially fully hermetically sealed on the top thereof by glass ~~coating~~ layer 30, on the bottom thereof by glass coating 40, and all edges thereof by the combination of the glass ~~coatings~~ layer 30 and the glass coating 40. As shown, a bond pad 14 having circuitry 16 connected thereto and substantially hermetically sealing the same is connected to a lead 62 of the conventional lead frame 60 by a suitable wire connection 66 having one end thereof 68 connected to the circuitry 16 connected, in turn, to bond pad 14 of semiconductor chip 12, while the other end 70 of the wire 66 is connected to the lead 62 of conventional lead frame 60. The semiconductor chip 12 is secured to or mounted on the paddle 64 of the conventional lead frame 60. Alternatively, the lead 62 of the conventional lead frame 60 may extend over (not shown) the semiconductor chip 12 for a typical lead-over-chip arrangement well known in the art with the wires 66 attaching the circuitry 16 to the lead 62 in such a manner.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] The third step of the present invention occurs when the active circuitry side of the semiconductor chips 12, while still in the form of a wafer 10, is coated with a suitable etchable glass ~~coating~~ layer 30. As previously stated, the etchable glass ~~coating~~ layer 30 may be of any desired suitable glass, preferably an etchable glass which cures at a relatively low temperature during processing, such as at a temperature of less than six hundred degrees Centigrade (600° C).

Please replace paragraph number **[0043]** with the following rewritten paragraph:

[0043] As the fifth step in the method of the present invention, a coating of suitable resist material is applied to the lower surface of the wafer 10 so that a portion of the street areas 22 located between the individual semiconductor chips 12 on the wafer 10 may be subsequently etched therethrough to the glass ~~coating~~ layer 30 on the top of the wafer 10. Any

suitable resist material may be used for such an etching process, depending upon the desired process parameters.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] As the sixth step of the present invention, after the resist coating has been applied to the bottom of the wafer 10 and cured, portions of the street areas 22 located between the semiconductor chips 12 of the wafer 10 are etched therethrough until the wafer 10 has been substantially etched through to the glass ~~coating~~ layer 30 applied to the active circuitry side (top or first side) of the wafer 10 with care being taken not to substantially etch through the glass ~~coating~~ layer 30. Any suitable etching process may be used, depending upon the material from which the wafer 10 is formed, such etching processes being well known in the art.

Please replace paragraph number **[0046]** with the following rewritten paragraph:

[0046] As the eighth step of the present invention, the bottom or second side of the wafer 10 is next coated with a suitable glass coating 40 to cover the bottom or second side of the wafer 10 and fill the previously etched portions of the street areas 22 located between the plurality of semiconductor chips 12 of the wafer 10. Any suitable glass coating may be used for such coating of the wafer 10 to provide a uniform, planar coating of glass on the bottom of the wafer 10. The glass coating 40 must extend through the portions of the street areas 22 previously etched, thereby contacting the glass ~~coating~~ layer 30 to form an area of glass replacing the portions of the wafer 10 which have been etched away. In this manner, the wafer 10 has effectively been reformed or recreated by the glass ~~coatings~~ layer 30 and the glass coating 40 filling the portions of the street areas 22 etched away.

Please replace paragraph number **[0047]** with the following rewritten paragraph:

[0047] The ninth step of the method of the present invention comprises applying a coating of suitable resist material on the active circuitry side (top or first side) of the semiconductor chips 12 over the glass ~~coating~~ layer 30 on the wafer 10, leaving the bond pad

areas 14 of the semiconductor chips 12 free of resist material. Any suitable resist material may be used, depending upon the desired process parameters of the etching process to be used.

Please replace paragraph number **[0048]** with the following rewritten paragraph:

[0048] As the tenth step of the method of the present invention, subsequent to applying the resist coating over the glass ~~coating~~ layer 30, the glass ~~coating~~ layer 30 is etched through to uncover predetermined bond pad areas 14 of each semiconductor chip 12 of the wafer 10. Any suitable etching process may be used, depending upon the type of glass ~~coating~~ layer 30 applied to the active circuitry side of the wafer 10.

Please replace paragraph number **[0049]** with the following rewritten paragraph:

[0049] As the eleventh step of the method of the present invention, after etching the glass ~~coating~~ layer 30 over the bond pads 14 of the semiconductor chips 12, the resist coating is removed from the glass ~~coating~~ layer 30, leaving the bond pads 14 exposed.

Please replace paragraph number **[0050]** with the following rewritten paragraph:

[0050] As the twelfth step of the method of the present invention, the glass ~~coating~~ layer 30 and exposed bond pads 14 of the semiconductor chips 12 are coated with a suitable metal coating which is compatible with the metal of the bond pads 14 of the semiconductor chips 12. If desired, before the bond pads 14 are coated with a metal coating, the bond pads 14 may have a diffusion barrier metal layer applied thereto followed by the application of the metal coating. The diffusion barrier metal layer may be applied by well known techniques and may be any suitable metal such as tungsten or metal alloys such as titanium-tungsten, titanium nitride, and the like. The metal coating may be applied by any suitable technique to the glass ~~coating~~ layer 30 and bond pads 14, such as by sputtering, etc. In this manner, the metal coating substantially hermetically seals the bond pads 14 of the semiconductor chips 12 and forms electrical contact therewith.

Please replace paragraph number **[0051]** with the following rewritten paragraph:

[0051] As the thirteenth step of the method of the present invention, a coating of suitable resist material is applied to the metal coating applied over the glass ~~coating~~ layer 30 of the semiconductor chips 12 of the wafer 10 with the resist material applied in the desired pattern to etch away the metal coating in the areas where paths for circuits 16 are not desired for connection to the bond pads 14 of each semiconductor chip 12. Examples of such circuits 16 remaining after the etching of the metal coating applied to the glass ~~coating~~ layer 30 and bond pads 14 are shown in drawing Figs. 2 through 4 hereinabove previously described.

Please replace paragraph number **[0053]** with the following rewritten paragraph:

[0053] As the fifteenth step of the method of the present invention, the resist material is then removed from the metal coating on the glass ~~coating~~ layer 30 on the semiconductor chips 12 of the wafer 10 to expose the circuits 16 electrically connected to and hermetically sealing the bond pads 14 of the semiconductor chips 12.

Please replace paragraph number **[0054]** with the following rewritten paragraph:

[0054] As the sixteenth step of the method of the present invention, portions of the street areas 22 located between the semiconductor chips 12 of the wafer 10 are sawed through at locations 50 in the street areas 22 so that glass ~~coatings~~ layer 30 and the glass coating 40 are maintained on the edges of each semiconductor chip 12 and the active circuitry (top or first) side of the semiconductor chip 12 and the bottom (second side) of the semiconductor chip 12, thereby substantially hermetically sealing the semiconductor chip 12 in glass while the bond pads 14 are substantially hermetically sealed by the metal coating forming the desired circuits 16 connected thereto. In this manner a plurality of semiconductor chips 12 have been formed with each semiconductor chip 12 being substantially fully hermetically sealed on each side thereof and on each edge thereof and the bond pads 14 being substantially hermetically sealed by the metal coating forming the circuits 16 to prevent environmental corrosion thereof without the use of a separate package. By using the method of the present invention to substantially fully

hermetically seal the semiconductor chip 12, without the use of a separate package, the semiconductor chip 12 of the present invention is of minimum size and occupies a minimum volume. Also, the semiconductor chip 12 formed by the method of the present invention has a desired configuration of circuitry connecting the bond pads 14 of the semiconductor chip 12 to a desired connector configuration which may include conventional lead frames 60 or lead-over-chip frames. If connected to lead frames, the semiconductor chip 12 of the present invention which is fully hermetically sealed in glass ~~coatings~~ layer 30 and the glass coating 40 may be subsequently packaged in suitable plastic materials in a conventional manner for further protection from damage. If desired, since the semiconductor chips 12 are substantially fully hermetically sealed by glass ~~coating~~ layer 30, having the desired circuitry 16 thereon, and glass coating 40, the semiconductor chips 12 may be directly inserted into mating connectors which match the circuitry formed on the semiconductor chips 12.